



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

HN

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,898	04/02/2001	Eric B. Kushnick	CRED 2164	2197
7812	7590	04/11/2005	EXAMINER	
SMITH-HILL AND BEDELL 12670 N W BARNES ROAD SUITE 104 PORTLAND, OR 97229			CHEN, TSE W	
			ART UNIT	PAPER NUMBER
			2116	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/824,898	KUSHNICK, ERIC B.
	Examiner Tse Chen	Art Unit 2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 February 2005.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-38 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-38 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date .

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____ .

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Remarks dated February 22, 2005.
2. Claims 1-38 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Re Claims 1-8, 11,15-16,20-27, 30, and 34-35

4. Claims 1, 3-4, 6-8, 11, 15-16, 20, 22-23, 25-27, 30, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyne, U.S. Patent 6194928, in view of Hondeghem, U.S. Patent 4255790, and Lu, U.S. Patent 6100735.
5. In re claim 1, Heyne discloses an apparatus [delay unit T] for generating pulses of a third pulse sequence [OUT] in response to pulses of a periodic first pulse sequence [IN] having a period T_p , wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period T_p [fig.1; summary of invention; adjustment resolution of delays have to be less than T_p in order to “incrementally” adjust until desired delay is reached], the apparatus comprising:

- First means [delay elements I_1 with mux1] to generate each second pulse [output from mux1] in response to a separate pulse of the first pulse sequence with a first delay adjustable by a first control data [first control line 1] and a resolution of T_p/N [t_1] over a

first range [12t1] substantially wider than Tp/M [t2], wherein M [3] and N [12] are differing integers greater than one [fig.3; col.3, 1.41 – col.4, 1.38; 12t1 = 3t2 where 12t1 is wider than t2].

- Second means [delay elements I2 with mux2] to generate each third pulse in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data [second control line 2] with a resolution of Tp/M [t2] over a second range [3t2] substantially wider than Tp/N [t1] [fig.3; col.3, 1.41-col.4, 1.38; 3t2 is wider than t1].
- A programmable sequencer [control unit CTR and phase detector; CTR is programmable with up/down controls from phase detector and in the broadest sense, programmed relating to the sequence of steps depicted in fig.3 to arrive at the appropriate configuration of delay elements] for changing a magnitude of the first control data and a magnitude of the second control data [control driven by CTR to each mux in determining the number of delay elements to be utilized represents the magnitude for each respective means] in response to each pulse of the first pulse sequence [phase detector generates up/down control to CTR in response to first pulse IN] such that the magnitudes of the first and second control data vary in a programmably adjustable manner [fig.1-3; col.4, 1.39 – col.5, 1.21].

6. Lu *concretely* affirms Heyne's teachings as discussed above in reference to the means [buffers 12] having resolutions [ICLK period/N] related to the period [ICLK period] [col.1, 1.36-col.2, 1.17; *prior art* illustrates, as is practical, that delay elements are related to period].
7. Hayne did not disclose that the programmable sequencer may vary the magnitudes in a repetitive fashion.

8. Hondeghem discloses an apparatus [fig.1] for generating pulses of a pulse sequence [A1-E1] in response to pulses of a periodic first pulse sequence [76] having a period T_p [abstract], the apparatus comprising:

- A programmable sequencer [CPU 70, RAM 84, I/O logic 112 with other associated circuitries] for changing a magnitude of the first control data [116] and a magnitude of the second control data [118] in response to each pulse of the first pulse sequence [76] such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner [fig.2-3; col.4, 1.62 – col.5, 1.57; col.6, ll.20-57; program X# of times for desired repetition].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Hayne and Hondeghem before him at the time the invention was made, to modify the apparatus disclosed by Hayne to include the programmable sequencer disclosed by Hondeghem, in order to obtain the programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way for performing tests that require various programmable repetitive sequences of pulse generation [col.1, ll.26-62].

10. As per claim 3, Heyne discloses at least one of the first and second ranges to be wider than T_p [abstract; fig.1-3; the second delay unit comprises of coarse delay elements that are used initially to increment the delay time to the range of the desired delay period, when the desired delay period is exceeded, a coarse delay element is removed and subsequent adjustments are performed with the first delay unit with finer delay elements, ergo, an ordinary artisan would

have inferred that the second delay unit must be designed with a range wider than the expected T_p in order for the initial adjustment to be performed correctly].

11. As per claim 4, Heyne discloses the first range is at least as wide as $(1-1/N)T_p$ and the second range is at least as wide as $(1-1/M)T_p$ [abstract; fig.1-3; both delay circuits have at least T_p and $5/3 T_p$ ranges, respectively, since T_p/N and T_p/M are integer fractions].

12. As per claim 6, Heyne discloses the generated third pulse sequence to be periodic [col.2, ll. 4-5].

13. As per claim 7, Heyne discloses a plurality of first gates [inverters or delay elements I1] connected in series for generating second pulses in response to first pulses wherein each first gate has a switching delay of T_p/N [fig.1; col.3, l.50].

14. As per claim 8, Heyne discloses a plurality of second gates [inverters or delay elements I2] connected in series for generating third pulses in response to second pulses wherein each second gate has a switching delay of T_p/M [fig.1; col.3, ll.51-52].

15. As per claims 11 and 16, Heyne discloses the apparatus wherein:

- The first means comprises a plurality of first gates [I1] connected in series for generating pulses of the second pulse sequence in response to first pulses wherein each first gate has a switching delay of T_p/N [fig.1; col.3, l.50].
- The second means comprises a plurality of second gates [I2] connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence wherein each second gate has a switching delay of T_p/M [fig.2; col.3, ll.51-52].

16. In re claim 15, Heyne discloses an apparatus [delay unit T] for generating pulses of a third pulse sequence [OUT] in response to pulses of a periodic first pulse sequence [IN] having a period T_p , wherein timing of each pulse of the third pulse sequence is adjustable with a

resolution that is smaller than period T_p [fig.1; summary of invention; adjustment resolution of delays have to be less than T_p in order to “incrementally” adjust until desired delay is reached], the apparatus comprising:

- First means [delay elements I_1 with mux1] to generate each second pulse [output from mux1] in response to a separate pulse of the first pulse sequence with a delay adjustable by a first control data [first control line 1] with a resolution of T_p/N [t_1] [fig.3; col.3, 1.41 – col.4, 1.38].
- Second means [delay elements I_2 with mux2] to generate each third pulse in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data [second control line 2] with a resolution of T_p/M [t_2] [fig.3; col.3, 1.41-col.4, 1.38].
- A programmable sequencer [control unit CTR and phase detector; CTR is programmable with up/down controls from phase detector and in the broadest sense, programmed relating to the sequence of steps depicted in fig.3 to arrive at the appropriate configuration of delay elements] for changing a magnitude of the first control data and a magnitude of the second control data [control driven by CTR to each mux in determining the number of delay elements to be utilized represents the magnitude for each respective means] in response to each pulse of the first pulse sequence [phase detector generates up/down control to CTR in response to first pulse IN] such that the magnitudes of the first and second control data vary in a programmably adjustable manner [fig.1-3; col.4, 1.39 – col.5, 1.21].

17. Hayne did not disclose that the programmable sequencer may vary the magnitudes in a repetitive fashion.

18. Hondeghem discloses an apparatus [fig.1] for generating pulses of a pulse sequence [A1-E1] in response to pulses of a periodic first pulse sequence [76] having a period T_p [abstract], the apparatus comprising:

- A programmable sequencer [CPU 70, RAM 84, I/O logic 112 with other associated circuitries] for changing a magnitude of the first control data [116] and a magnitude of the second control data [118] in response to each pulse of the first pulse sequence [76] such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner [fig.2-3; col.4, 1.62 – col.5, 1.57; col.6, ll.20-57; program X# of times for desired repetition].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Hayne and Hondeghem before him at the time the invention was made, to modify the apparatus disclosed by Hayne to include the programmable sequencer disclosed by Hondeghem, in order to obtain the programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way for performing tests that require various programmable repetitive sequences of pulse generation [Hondeghem: col.1, ll.26-62].

20. In re claims 20, 22-23, 25-27, 30, and 34-35, Heyne, Lu and Hondeghem disclose apparatus; therefore, Heyne, Lu and Hondeghem disclose method of operating apparatus.

Re Claims 2, 5, 21, 24

21. Claims 2, 5, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyne, Lu and Hondeghem as applied to claims 1, 4, 20 and 23 above, and further in view of Gorbics et al., U.S. Patent 5838754, hereinafter Gorbics.
22. Heyne, Lu and Hondeghem disclose each and every limitation of the claims as discussed above in reference to claim 1, 4, 20 and 23. Heyne, Lu and Hondeghem did not disclose explicitly that M and N are relatively prime.
23. Gorbics discloses an apparatus [fig.2; time interval measuring device] wherein M [delay elements N] and N [harmonic H] are relatively prime [col.4, ll.19-50].
24. It would have been obvious to one of ordinary skill in the art, having the teachings of Gorbics, Hayne, Lu and Hondeghem before him at the time the invention was made, to modify the apparatus discloses by Hayne, Lu and Hondeghem to include the teachings of Gorbics, in order to obtain the apparatus wherein M and N are relatively prime. One of ordinary skill in the art would have been motivated to make such a combination in order to not be limited by the resolution of the delay elements [Gorbics: col.2, ll.11-20, ll.55-65; col.4, ll.28-50].

Re Claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38

25. Claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyne, Lu and Hondeghem as applied to claims 8, 11, 16, 27, 30 and 35 above, and further in view of Liedberg, U.S. Patent 5471165.
26. Heyne, Lu and Hondeghem disclose each and every limitation of the claims as discussed above in reference to claims 8, 11, 16, 27, 30 and 35. In particular, Heyne discloses an integrated pulse delay device comprising of two delay units wherein the units comprises of gates connected

in series for generating a range of delay periods that can be monitored to produce the appropriate control signals for phase-locking the first input and final output pulses [fig.2].

27. However, Heyne and Hondeghem did not disclose an extra series of gates for the delay units or a way to monitor and phase-lock the first input pulse sequence with the output pulse sequence from the first gates.

28. Liedberg taught a modular signal processing circuit with means to delay a periodic input signal by utilizing a multitude of delay gates and means to monitor and phase-lock the input and output pulses [fig.2; col.4, ll.5-35].

29. In re claims 9, 12, and 17, Liedberg taught the modular pulse delay unit comprising of:

- M third gates [delay device D2] connected in series with second gates [delay device D1] for generating a fourth pulse sequence in delayed response to the first pulse sequence [fig.2; col.3, ll.57-58; col.4, ll.29-35].
- Wherein each second and third gate has a similar switching delay of T_p/M set by the magnitude of a second control signal applied to all the second and third gates [col.4, ll. 24-35; col.5, ll.31-40].

30. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to increase the resolution and accuracy of a pulse delay generating device [Liedberg: col.1, ll.24-28; col.2, ll.48-54, ll.63-64].

31. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Heyne and Liedberg to provide a pulse delay generating device with a multitude of delay gates connected in series within a phase monitoring and locking system to increase the resolution and accuracy of the generated pulses.

32. As per claims 10, 13, and 18, Heyne taught the monitoring of a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the first control signal so that the fourth pulse sequence is phase-locked with the first pulse sequence [fig. 2].

33. As per claims 14 and 19, Liedberg taught the modular pulse delay unit comprising of:

- Plurality of first N gates [delay device D1] connected in series for generating a pulse sequence in delayed response to the first pulse sequence [fig.2; col.3, ll.57-58; col.4, ll. 29-35].
- Wherein each gate has a switching delay set by the magnitude of a first control signal [col.4, ll.24-35; col.5, ll.31-40].
- Wherein the first pulse sequence and the generated pulse sequence are monitored and the first control signal is adjusted to phase lock the pulse sequences [col.4, ll.5-35].

34. As per claims 28-29, 31-33, and 36-38, Heyne, Lu, Hondeghem, and Liedberg taught apparatus; therefore, Heyne, Lu, Hondeghem, and Liedberg taught method of operating apparatus.

Response to Arguments

35. Applicant's arguments filed February 22, 2005 have been fully considered but they are not persuasive.

36. Applicant alleges that Examiner "reforms" or "rewrites" the "previous Office Action to state that the input period T_p is 'delayed' by the number of N or M delay elements rather than 'adjusted'". Examiner reminds Applicant that Examiner was merely attempting to clarify a less

accurate term [“delayed” is a more specific term than the broader “adjusted”] for Applicant’s benefit.

37. Applicant devotes the majority of the argument in maintaining that Heyne “does not teach or suggest that the delay of either I1 or I2 should have any relationship to the period T_p of the signal being delayed, and in particular does not teach that they should be fixed functions T_p/N and T_p/M of the period T_p of the input signal as recited in claim 1”. Examiner likewise maintains the position set forth in previous Office Actions. However, in the interest of moving the prosecution forward, Examiner has provided new ground(s) of rejection based on Lu as discussed above [Lu provides evidence that related prior art do indeed establish the relationship between the delay elements and the input period]; thus, rendering Applicant’s arguments [pages 2-8] moot.

38. Applicant alleges that “Examiner’s comments to part 3 of Applicant’s reply to the final Office Action... the example cited by the Examiner ($N=1$ and $M=4$) does not meet the terms of claims 1, 20 or 34, each of which requires that both M and N be greater than one, and does not meet the requirement of claims 2, 5, 21, 24, or 34 that M and N be relatively prime”. Firstly, Examiner is perplexed as to why Applicant continues to assert that 1 and 4 are not considered relatively prime when Applicant’s own disclosure teaches that two numbers are relatively prime if they have no common *factors* other than 1 [i.e., the factors of 4 are 1, 2, and 4 while the factor for 1 is 1]. Secondly, Applicant’s argument is out of context in regards to claims 1, 20 or 34 as Examiner cited Applicant’s derived values ($N=1$ and $M=4$) to support the rejection of claims 2, 5, 21, 24, or 34 that M and N be relatively prime. Applicant may not have understood Applicant’s own elegant derivation to be a ratio between M and N . Examiner reminds Applicant that ratios don’t necessarily represent the actual numbers, which in the instant case, are

represented by 5[N] and 12[M] in figure 3. Again, in the interest of moving the prosecution forward, Examiner has provided new ground(s) of rejection based on Gorbics as discussed above (“relatively prime” is explicitly stated); thus, rendering Applicant’s arguments moot.

39. In response to applicant’s argument that “the rejection of the claims over the combination of Heyne and Hondeghem are correct in both form and substance”, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the instant case, it would have been obvious to one with ordinary skill in the art to incorporate the “repetitive waveform” teachings of Hondeghem with the apparatus disclosed by Heyne, in order to obtain the programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner.

40. Applicant alleges that Liedberg fails “to teach the additional elements of claim 9”. Examiner maintains that the combination of Heyne, Hondeghem and Liedberg discloses the additional elements of claim 9. Again, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. In the instant case, it would have been obvious to one of the ordinary

Art Unit: 2116

skill in the art to incorporate the teachings of Liedberg with the apparatus disclosed by Heyne and Hondeghem and in effect, satisfying the additional elements of claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
April 1, 2005



JOHN R. COTTINGHAM
PRIMARY EXAMINER